作业批改链接
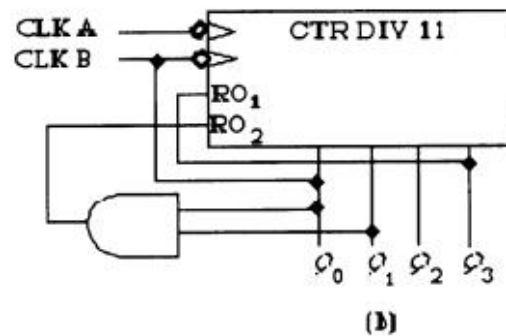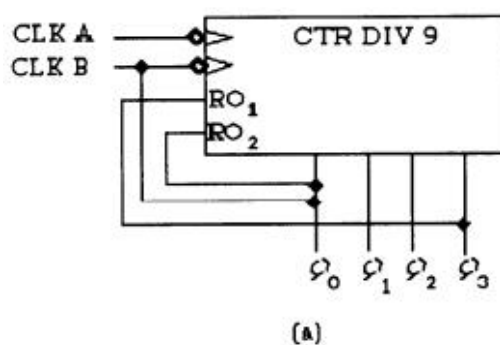
Homework 6

Due 14:20, Tuesday @ Week 12

"Digital Fundamentals", **11th Edition**

Chapter 9, Problems

6(a)(b)，10，12，16，18，22，24(d)
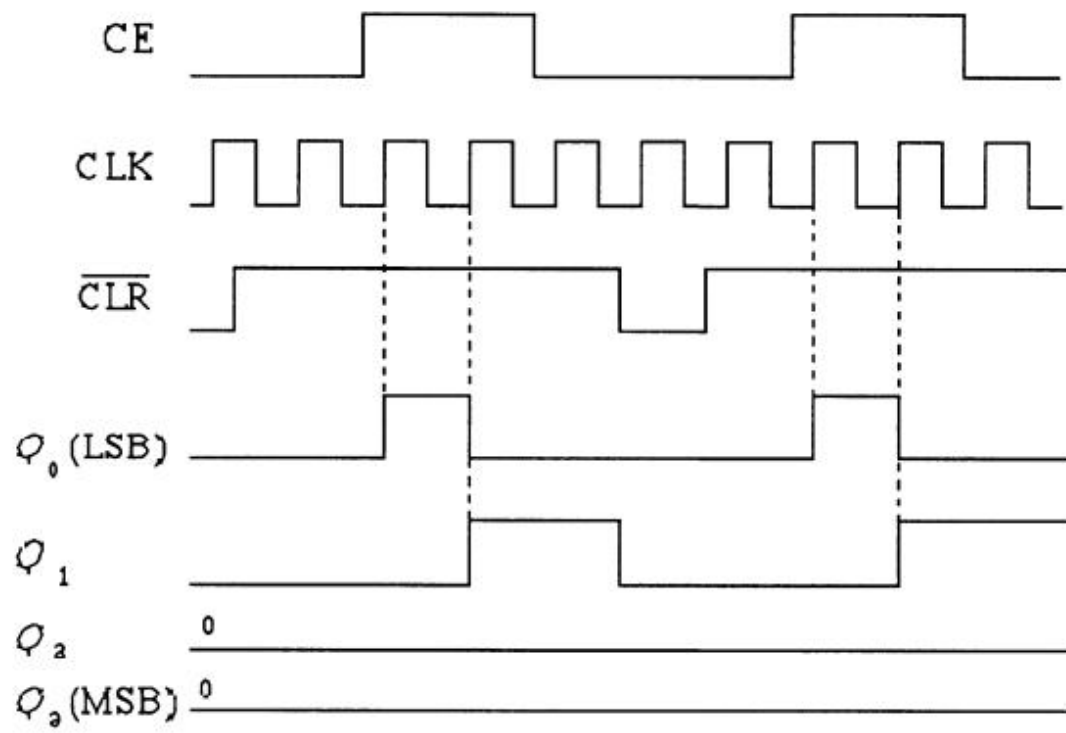
Make sure that the output diagram is aligned with the input diagram.

T6(a)(b)

(a)   (b)

1001、1011

T10

T12
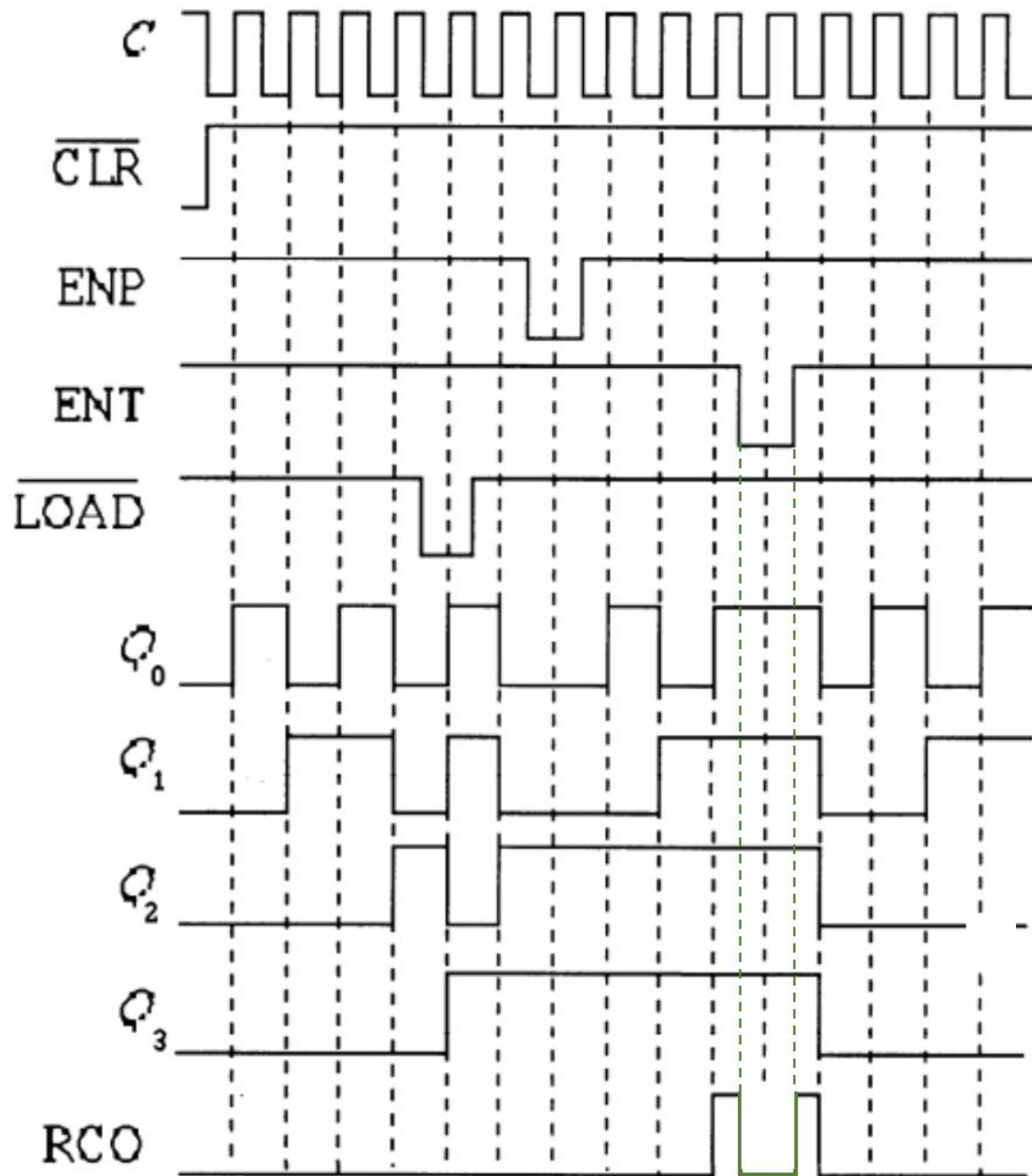
RCO = ENT AND Q0 AND Q1 AND Q2 AND Q3.
Note: The RCO is a combinational logic output and is independent of the clock.

T16

16. Repeat Problem 15 if the D/$\overline{U}$ input signal is inverted with the other inputs the same.

15. Develop the *Q* output waveforms for a 74HC190 up/down counter with the input waveforms shown in Figure 9–72. A binary 0 is on the data inputs. Start with a count of 0000.
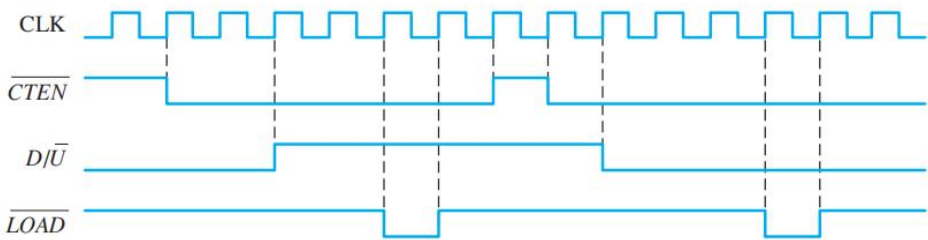

FIGURE 9–72

Note 1: The 74HC190 is a decade (decimal) counter. The maximum value of Q is 9
Note 2: Edge-triggered devices respond to the input levels present just before the clock edge.

The values of Q at fifteen rising edges are as follows:

$\overline{CTEN}$	$\overline{CTEN}$	-1	-1	+1	+1	$\overline{LOAD}$	+1	$\overline{CTEN}$	+1	-1	-1	-1	$\overline{LOAD}$	-1
0	0	9	8	9	0	0	1	1	2	1	0	9	0	9

T18

	Q_2	Q_1	Q_0	D_2	D_1	D_0
Initially	0	0	0	0	0	1
At CLK 1	0	0	1	0	1	1
At CLK 2	0	1	1	1	1	1
At CLK 3	1	1	1	1	1	0
At CLK 4	1	1	0	1	0	0
At CLK 5	1	0	0	0	0	1
At CLK 6	0	0	1	0	1	1

The sequence is 000 to 001 to 011 to 111 to 110 to 100 and back to 001, etc.

$$D_0 = \overline{Q_0 \cdot Q_1}$$

$$D_1 = Q_0$$

$$D_2 = Q_1$$

$$Q_0^+ = D_0 = \overline{Q_0 \cdot Q_1}$$

$$Q_1^+ = D_1 = Q_0$$

$$Q_2^+ = D_2 = Q_1$$

T22

NEXT-STATE TABLE

Present State				Next State			
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	1	0	0	1
1	0	0	1	0	0	0	1
0	0	0	1	1	0	0	0
1	0	0	0	0	0	1	0
0	0	1	0	0	1	1	1
0	1	1	1	0	0	1	1
0	0	1	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	0	0	0

TRANSITION TABLE

Output State Transition (Present State to next state)				Flip-flop Inputs							
Q_3	Q_2	Q_1	Q_0	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
0 to 1	0 to 0	0 to 0	0 to 1	1	X	0	X	0	X	1	X
1 to 0	0 to 0	0 to 0	0 to 1	X	1	0	X	0	X	X	0
0 to 1	0 to 0	0 to 0	1 to 0	1	X	0	X	0	X	X	1
1 to 0	0 to 0	0 to 1	0 to 0	X	1	0	X	1	X	0	X
0 to 0	0 to 1	1 to 1	0 to 1	0	X	1	X	X	0	1	X
0 to 0	1 to 0	1 to 1	1 to 1	0	X	X	1	X	0	X	0
0 to 0	0 to 1	1 to 1	1 to 0	0	X	1	X	X	0	X	1
0 to 0	1 to 1	1 to 0	0 to 0	0	X	X	0	X	1	0	X
0 to 0	1 to 1	0 to 0	0 to 1	0	X	X	0	0	X	1	X
0 to 0	1 to 0	0 to 0	1 to 0	0	X	X	1	0	X	X	1

Binary states for 10, 11, 12, 13, 14, and 15 are unallowed and can be represented by don't cares.

$J_3 = \overline{Q_2}\,\overline{Q_1}$

$J_2 = Q_1$

$J_1 = Q_3\overline{Q_0}$

$J_0 = \overline{Q_3}\,\overline{Q_2} + \overline{Q_3}\,\overline{Q_1}$

$K_3 = 1$

$K_2 = Q_0$

$K_1 = Q_2\overline{Q_0}$

$K_0 = \overline{Q_3}\,\overline{Q_2} + \overline{Q_3}\,\overline{Q_1}$

T24(d)

$$\text{Modulus} = 2 \times 4 \times 6 \times 8 \times 16 = \mathbf{6144}$$

$$f_1 = \frac{39.4\,\text{kHz}}{2} = \mathbf{19.7\,kHz}$$

$$f_2 = \frac{19.7\,\text{kHz}}{4} = \mathbf{4.925\,kHz}$$

$$f_3 = \frac{4.925\,\text{kHz}}{6} = \mathbf{820.83\,Hz}$$

$$f_4 = \frac{820.683}{8} = \mathbf{102.6\,Hz}$$

$$f_5 = \frac{102.6\,\text{kHz}}{16} = \mathbf{6.41\,Hz}$$